areas for gate electrodes;

lightly doped source/drain areas with said second conductive type dopant in said device areas adjacent to said gate electrodes and an insulating sidewall spacers on the sidewalls of said gate electrodes;

heavily doped first source/drain contact areas composed of said second conductive type dopant in said device areas adjacent to said insulating sidewall spacers;

a silicide layer on said gate electrodes and on said source/drain contact providing said Salicide field effect transistors;

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a conformal barrier layer, and an interlevel dielectric layer on said Salicide field effect transistor;

borderless contact openings in said interlevel dielectric layer and said barrier layer to said source/drain areas and extending over said field oxide with unintentional over-etched field oxide regions at said field oxide-source/drain area interface;

a dopant composed of said second conductive type in said substrate under and adjacent to said over-etched field oxide regions in said borderless contact openings providing said source/drain contact areas with a continuous doped region around said over-etched field oxide regions.